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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,478	NEMECEK ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 December 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/18/06*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 were rejected in Office Action dated 24 October 2005. Applicants' response dated 22 December 2005 has amended claims 1, 3, 10, 12, 14, and 19, and cancelled claim 11. Claims 1-10 and 12-21 have been submitted for reconsideration.

Claims 1-10 and 12-21 have been rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Claim Objections

2. Applicant is advised that should claim 2 (or claim 13) be found allowable, claim 3 (14) will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims

in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

This notice is applied in light of the definition of "register", supplied in the previous Office Action, as known in the art. The terms "memory" and "register" are generally synonymous, however specialized forms of either could be distinguished from each other. If Applicant believes the disclosure adequately distinguishes between the term "register" and "memory", clarification is requested including specific citation of those portions of the specification as filed which support that distinction.

In response, Applicants argue primarily that:

> Applicants respectfully assert that this definition [provided by the Examiner in the previous action] is unreasonably broad, as it includes devices clearly outside the scope of the present invention (e.g., punch cards).
>
> As such, Applicants respectfully submit that the following definition from Wikipedia [hyperlink omitted] is a more appropriate definition of the term "register" as it is commonly used today by those skilled in the art [quotation omitted]. As stated in response to the prior Office Action, "memory" is a term referring generally to many different types of storage for a digital system, whereas "register" is a more specialized term generally referring to high-speed memory within a processor or other electronic device, used to hold data for a particular purpose. Thus, Applicants respectfully submit that "memory" and "register" are not synonymous, thereby rendering distinguishable Claims 2 and 3, and Claims 13 and 14.

The Examiner respectfully traverses this argument as follows.

The dependability of Wikipedia, "the free encyclopedia that anyone can edit" (see "Main Page – Wikipedia," cited on form PTO-892) should not be overlooked. Applicants have not supplied a printout of the specific Wikipedia pages to which they have referred. At present, the page appears to have been last modified on 26 February 2006, more than two months after Applicants' current response, and has apparently been modified at least 12 separate times in the

interim. The Examiner respectfully requests that Applicants provide a printout, including the date when that printout was retrieved from the Internet, when referring to a reference that is "written collaboratively by many of its readers."

Regardless, the "Processor register" page cited by Applicants does not appear to fully support Applicants' argument. Indeed, the definition provided by Wikipedia is at best vague and indefinite: "a **small amount** of **very fast** computer memory used to speed the execution of computer programs by providing **quick access to commonly used values – typically**, the values being in the midst of a calculation at a given point in time." Based on this definition, how can one tell a register from memory? How does this definition distinguish, for example, claim 2 from claim 3 such that both claims comply with 35 U.S.C. § 112, second paragraph? Wikipedia defines a register as memory, in complete accordance with IEEE 100, and is the basis for this rejection.

It is unclear how Applicants' desire the information from Wikipedia to be read into the claims. It appears that Applicants' intend for the term "register" in claim 2 to be interpreted as "smaller, faster memory than that of claim 3," where claim 3 recites no limitations regarding size or speed. This is clearly improper claim language.

Where claims 3 and 14 have been amended to recite that the memory is "coupled" to the processor, the Examiner respectfully submits that the registers of claims 2 and 13 are also "coupled" to the processor, else several significant issues under 35 U.S.C. §§ 101 and 112, first paragraph, (such as utility, operability, enablement, and written description) must be addressed. Therefore, until Applicants make an express statement to the contrary, the Examiner interprets

both the register of claim 2 and the memory of claim 3 as "coupled" to the processor. Therefore, this language does not distinguish the claims.

Applicants' arguments have been fully considered but have been found unpersuasive. The previous interpretation that claims 2 and 3 (13 and 14) are substantially identical is maintained.

IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition (2000) provides the following definitions:

- **memory (1)** All of the addressable storage in a processing unit and other internal storage that is used to execute instructions.
- **register (1)** A device capable of retaining information, often that contained in a small subset (for example, one word), of the aggregate information in a digital computer.
- **register (4)** A storage device or storage location having a specified storage capacity.

Claim Rejections - 35 USC § 112

The previous rejections of claims 12-21 under 35 U.S.C. § 112 have been withdrawn in response to Applicants' amendments of claims 12 and 19.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 3, 13, and 14 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 2 and 3, as explained above Applicants' arguments apparently define the term "register" in claim 2 to be interpreted as "smaller, faster memory than that of claim 3," where claim 3 recites no limitations regarding size or speed. This claim language and interpretation is vague and indefinite because, where claim 3 presents no limitations regarding size or speed, it is impossible determine what, if anything, in the prior art meets the limitations of claim 2. Further, the terms "smaller" and "faster" are relative terms that are defined neither in the claims nor the application as filed.

It is clear from Applicants' response that claims 2 and 3 should be interpreted as separate and distinct definitions of the claimed invention, however these definitions are vague and indefinite.

Claims 13 and 14 recite limitations corresponding to claims 2 and 3, respectively, and are rejected for similar rationale.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 10, and 12 are rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,371,878 to Coker.

Regarding claims 1 and 12, Coker discloses a method of executing code in a microcontroller ("Embedded Computer System or ECS", see column 1, lines 20-23) [*"[T]his invention uses hardware and software which can 'shadow' the execution of a target-ECS in real time operation"* (column 2, lines 34-40)];

Executing a set of timing code to enable lock-step synchronization in a virtual microcontroller ("shadow system"), wherein the timing code is timed to take the same number of clock cycles as the microcontroller uses to execute boot code, [*"A shadow system of this invention executes the same software as the target-ECS from system start-up or reset."* (column 2, lines 56-58); *"The shadow system and the target-ECS function exactly the same except that the shadow system receives data slightly delayed because of a data buffer between the target-ECS and the shadow system."* (column 3, lines 13-16); *"[I]n terms of relative time, the execution state of the shadow system 28 at the time when any given instruction is executed will directly correspond to the execution state of the target-ECS when the same instruction was executed.."* (column 8, lines 44-49)];

Wherein the boot code is stored within the microcontroller and at least one portion of the boot code is inaccessible to the virtual microcontroller [Interface means 19 connecting the target-ECS and shadow system is used by Coker to transmit I/O data and does not appear to contain any suggestion that instruction code or boot code is transmitted via interface means. See (column 4, lines 9-18)]; and

Simultaneously halting both the microcontroller and the virtual microcontroller [the target-ECS and the shadow system execute the same code (column 2, lines 56-58) and execute at in lock-step synchronization (column 8, lines 44-49), therefore when the target-ECS halts, the shadow system simultaneously halts. It is inherent that a computer processor in a debugging system halts because there is a distinct conclusion to the debugging process. An infinitely executing debugging process would fail to achieve its explicit goal of validating the software or hardware].

Regarding claim 10, the rationale given above for claim 1 is incorporated and additionally Coker discloses resetting the microcontroller and the virtual microcontroller [*"A shadow system of this invention executes the same software as the target-ECS from system start-up or reset."* (column 2, lines 56-58)].

The claim recites "setting a break at assembly instruction line zero," and subsequently "simultaneously halting both the microcontroller and the virtual microcontroller by branching to assembly instruction line zero." The limitation of "assembly instruction line zero" appears to be an arbitrary location for setting the breakpoint.

Coker discloses copying register and memory contents from the microcontroller to corresponding registers and memory in the virtual microcontroller [*"[T]he shadow system receives its input data from the input registers of the target-ECS and stores in the input data in its RAM... Using the address of unique input events in a specially segregated portion of its RAM, the shadow system central processing unit (CPU) can perform numerical operations on the data*

with its microprocessor and similarly send outputs to specific locations within its RAM rather than to complex output registers." (column 2, line 63 – column 3, line 12)].

The limitation of "removing the break at assembly line zero after copying the register contents and copying the memory contents" is regarded as the necessary and inherent steps of practicing Coker's invention in order to debug the system. Merely halting execution is not sufficient to implement a debugging system, therefore removing a break is necessary to continue the debugging process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-10 and 12-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,202,044 to Tzori.

Regarding claims 1 and 12, Tzori teaches an emulation system having a microcontroller, effectively the device under test (DUT), operating in lock-step with a virtual microcontroller, effectively a virtual processor [*"The digital-logic simulation process and the hardware pod may operate in an engaged operating mode... stimulus/response process"* (column 5, lines 14-24)].

Tzori teaches executing code in the microcontroller (DUT) [*"stimulation-control data to be transmitted to the hardware pod 32 for stimulating a digital logic IC inserted into the IC socket 34"* (column 9, lines 33-37)]. The limitation of executing a "boot code" is regarded as an obvious detail of implementation as Tzori teaches executing instructions in general. Additionally, the "boot code" must be stored on the device under test in order for the device under test to execute that code.

Tzori teaches "executing timing code to enable the lock-step synchronization, wherein the timing code is timed to take the same number of clock cycles" is clearly taught by Tzori by virtue of the method performed by the simulation process and hardware pod [*"stimulus-response cycle"*; *"engaged mode"* (column 9, line 10 – column 10, line 39); *"disengaged mode"* (column

10, line 40 – column 11, line 8); *"re-enters the engaged operating mode"*; *"a delay may occur between transmission of response data from the hardware pod 32 to the simulation process 22, indicated by the line 162, and the resumption of engaged mode operation... Such a delay may occur while the simulation process 22 performs some portion of the digital logic simulation that must be completed before the simulation process 22 may re-enter the engaged operating mode"* (column 11, lines 9-33); Figs. 2 and 3]. When disengaging the hardware pod to execute a set of boot code, it would be obvious to a person of ordinary skill in the art that Tzori teaches that the simulation process must execute "timing code [...] timed to take the same number of clock cycles". That is, Tzori plainly suggests a combination of lock-step synchronization with "timing code" that allows the microcontroller and virtual processor to optionally disengage from each other [*"An advantage of the improved digital logic simulation/emulation system is that it frees the digital-logic simulation process and the hardware pod from operating in lock-step with each other at the stimulation/response cycle of the digital logic circuit."* (column 5, line 64 – column 6, line 1)].

Regarding the step of simultaneously halting, this step is well known in the art as a breakpoint for a concurrent process. In this instance, the concurrent processes are executing in parallel on separate devices (virtual microcontroller and microcontroller, or virtual processor and DUT). Tzori's system and method are clearly conducive to this type of breakpoint, achieved by using the control data during the engaged mode (or invoking the engaged mode if necessary) to simultaneously halt both the microcontroller and virtual microcontroller.

Tzori does not expressly state that the digital logic circuit 34 is a microcontroller. It would have been obvious to a person of ordinary skill in the art to use Tzori's system and method for the particular type of device being designed, whether a microcontroller, a processor, an ASIC, or some other form of integrated circuit logic device. The motivation to do so would be found in the teachings of Tzori as cited above as well as from the nature of the problem to be solved. The combination would be formed according to the teachings of Tzori, where the simulation process and digital logic IC taught by Tzori are modified to correspond to the integrated circuit digital logic device preferred by the designer.

In response, Applicants' argue primarily that:

> Applicants respectfully assert that whereas the claimed invention involves <u>running boot code in the microcontroller</u> amongst other operations to enable lock-step synchronization (line 28 of page 4 to line 9 of page 5), Tzori teaches <u>loading logic configuration data into devices other than the device under test</u> during the initialization interval. Thus, not only is the microcontroller as claimed very different from the configurable-logic ICs taught by Tzori, but the operations described (running code vs. loading data into) and the information involved (boot code vs. logic configuration data) are also very different.

The Examiner respectfully traverses this argument as follows.

Applicants' arguments are directed to column 9, lines 20-30 of Tzori as teaching the execution of boot code. This argument does not reflect the rejection as written. As stated above:

> "The limitation of executing a "boot code" is regarded as an obvious detail of implementation as Tzori teaches executing instructions in general. Additionally, the "boot code" must be stored on the device under test in order for the device under test to execute that code."

Although Tzori does not expressly disclose executing "boot code," Tzori does nonetheless teach execution of instructions. While the claims recite "boot code," there is no feature of "boot code," inherent, implicit, or explicit, which renders it somehow unique or novel over instructions in general. "Boot code" is merely a desirable combination of normal instructions for achieving a

particular purpose. As stated previously, where Tzori teaches the execution of instructions, it would have been obvious to a person of ordinary skill in the art to execute "boot code," in addition to other widely known types of code. In contrast, certainly Tzori does not suggest to a person of ordinary skill in the art that a random collection of meaningless instructions should be executed in order to test the device.

Additionally, it is unclear to which limitations Applicants refer by stating "not only is the microcontroller as claimed very different from the configurable-logic ICs taught by Tzori." Is this a separate argument?

Applicants' further argue that:

> Embodiments of the claimed invention disclose running timing code in the virtual microcontroller while the microcontroller simultaneously runs boot code to enable lock-step synchronization between the microcontroller and the virtual microcontroller (page 5, lines 2-9).

The Examiner respectfully traverses this argument as follows.

It is unclear whether Applicants are referring to the claimed invention or the disclosed invention. Nevertheless, Tzori's Figure 2 and related disclosure teaches the related limitations in claim 1.

Applicants also argue that:

> Moreover, by teaching the loading of logic configuration data into the devices other than the device under test to initialize the simulator, Tzori effectively teaches away from the claimed embodiments.

And

> As such, assuming arguendo that the simulation process and server process taught by Tzori are equivalent to the virtual microcontroller as claimed, Applicants respectfully assert that Tzori teaches away from running timing code as claimed given that Tzori instead teaches that the simulation process loads logic configuration data during the initialization interval.

The Examiner respectfully traverses this argument as follows.

The Examiner is unaware of support in the MPEP for the concept of "teaching away" as applied by Applicants. In order to comport with the MPEP, Tzori's teaching that "the simulation process loads logic configuration data" would need to be interpreted as meaning "not running timing code," and also interpreted as meaning "running timing code is undesirable and insufficient to practice the invention." The term "timing code" is, of course, extraordinarily broad, and there does not appear to be any support in Tzori to support Applicants' claims that Tzori somehow "teaches away." Is there any specific passage in Tzori that "timing code" is inferior?

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claims 2, 3, 13 and 14, Tzori teaches transmitting response data from the hardware pod (microcontroller or DUT) to the simulation process (virtual microcontroller or virtual processor) (column 11, lines 23-33). This step allows for the simulation process to perform "some portion of the digital logic simulation that must be completed before the simulation process may re-enter the engaged operating mode". It would be obvious to a person of ordinary skill in the art at the time of Applicants' invention that synchronizing the simulator process and hardware pod is necessary and performed at this step. As synchronization between the two devices means their registers (real or virtual) and memory contents hold the same values, it would be obvious to a person of ordinary skill in the art at the time of Applicants' invention to copy the register values and memory contents from one device to the corresponding register

values of the other, especially in light of Tzori's explicit teaching of data transfer between the two when re-entering the engaged operating mode.

Regarding claims 4, 5, 15 and 16, these claims are interpreted as meaning that both the microcontroller (DUT) and virtual microcontroller (virtual processor) branch to the beginning of a section of code following a breakpoint (the simultaneously halting step of claim 1). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to begin a second task at the beginning of that second task upon completion of a first task (boot code or otherwise) when using the system taught by Tzori. Branching to different points in code is extremely well known in the art. If Applicant intends the phrase "branches to assembly instruction line 0" to be read as a literal limitation, clarification is respectfully requested, however the specification (page 28, lines 5-8) appear to teach this phrase as an address stop as known in the art.

Regarding claims 6 and 17, official notice is taken that numerous methods of achieving data protection to effectively "hide data" are well known in the art. It would have been obvious to a person of ordinary skill in the art to hide the boot code from the virtual microcontroller to achieve the numerous advantages of data protection, many of which are known in the art. Applicants have not challenged this use of Official Notice and it is therefore considered admitted prior art. Please see MPEP 2144.03.

Regarding claims 7 and 18, these claims recite setting and initiating a breakpoint, as defined above and known in the art. Official notice is taken that breakpoints are well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to implement breakpoints as known in the art.

Claims 8 and 19 recite combinations of the limitations found in claims 2-4 and 7; and 13-15 and 18, respectively. As these claims are obvious in view of Tzori, as set forth above, different combinations of these limitations are similarly obvious in view of Tzori.

Claims 9 and 20 recite removing a breakpoint. Official notice is taken that removing a breakpoint is well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to remove a breakpoint if he no longer wanted execution to break at that instruction.

Claim 10 recites a combination of limitations found in claims 1, 8, and 9. As these claims are obvious in view of Tzori, as set forth above, different combinations of these limitations are similarly obvious in view of Tzori.

Claim 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tzori as applied to claim 12 above, and further in view of "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System" by Matthew Dahl, Jonathan Babb, Russel Tessier, Silvina Hanono, David Hoki, and Anant Agarwal (Dahl) and further in view of "A Reconfigurable Logic

Machine for Fast Event-Driven Simulation" by Jerry Bauer, Michael Bershteyn, Ian Kaplan, and Paul Vyedin (Bauer).

Tzori teaches that the simulation process (virtual processor) is implemented on a Sun workstation (column 6, line 63-65). Tzori does not explicitly teach that the simulation process is implemented on a field programmable gate array (FPGA).

Dahl teaches that it is known in the art to emulate a Sparc microprocessor using an FPGA (abstract).

Bauer teaches that hardware emulation can increase simulation speed by up to 10,000 times (introduction, paragraphs 1-2).

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine these teachings and arrive at the decision to implement the simulation process of Tzori, originally implemented on a Sun workstation, on an FPGA to realize an enormous increase in simulation speed. Knowledge that this was possible is provided by Dahl, and motivation to combine the references, to increase simulation speed, is provided by Bauer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 3/9/06
Supervisor Primary Examiner
Art Unit ~~2125~~ 2123